REMARKS

The allowance of claim 49 and the indication of allowability of claim 45 are appreciated. Claim 45 has been rewritten into independent form and should be in clear condition for allowance.

New claim 50 has been added and is similar in many respects to claim 18. Claim 50 further requires the source enable signal applied after the power to comprise a display erase command. Support in the specification for claim 50 is at page 40, for example.

The rejection of claims 18, 20, 23, 31, 33, 41 and 46 to 48 as being obvious over Yasui (U.S. Patent No. 5,248,963) in view of Tsuboyama et al (US Patent 5,592,191 – Tsuboyama) is traversed.

Independent claim 18 (on which all rejected claims depend) has been amended to require a selecting level that is applied "solely" to erase the display after the display has been turned OFF. The selecting level is applied only after power has been turned off. Yasui and Tsuboyama do not teach applying a source enable signal at a particular selecting level solely after power has been turned off, such that the selecting level causes a source driver to apply an OFF voltage as a video signal to erase the pixel electrodes.

I. SUMMARY

Independent claim 18 (and dependent claims 20, 23, 31, 33, 41 and 46 to 48) recites several elements that are not disclosed or suggested by Yasui and Tsuboyama including:

- Claim 18 as amended recites a "source enable signal which is at a selecting level solely during the certain period." The certain period is "after said power source is turned OFF". The support in the specification for a selecting level "only" applied after the power source is turned OFF is at page 40, for example. The specification states that the source enable signal is used to judge whether to apply an erase signal. As is noted in the Office Action at page 3, Yasui does not output a source enable signal at a selecting level after an OFF signal. Tsuboyama does not disclose a selecting level that is applied "solely" after an OFF signal.
- Claim 18 recites a "source driver", a "source driver control circuit", and a "power source control circuit" for the source driver. These circuit elements are not disclosed expressly or inherently in Yasui in the manner recited in claim 18. Contrary to the Action at page 6, there is no "inherent circuit" in Yasui that is the same as the claimed source driver, source driver control circuit and power source control circuit. In Figure 3 of Yasui, the "source bus drive circuit" (16) has inputs of: D, PCK, M, E_1, E_2, E_3 and EG. In

Figures 3 and 5, the "gate bus drive circuit" (17) has inputs of: Vcl, V_1', V_2', V_3, Hs and Vs. Given the differences in the inputs, it cannot be assumed that the circuit structure of the gate bus drive circuit is inherently the same as the circuit structure of the source bus drive circuit.

II. YASUI DOES NOT DISCLOSE A POWER SOURCE CONTROL CIRCUIT THAT APPLIES A "SELECTING LEVEL" TO CAUSE DISPLAY ERASURE

The Office Action (p. 3) correctly recognizes that Yasui does not teach the a power source control outputting a source enable signal at a selecting level that causes the source driver control circuit to erase the display. Contrary to the Action, it would not have been obvious to modify Yasui to have this feature.

Yasui discloses a method to erase a liquid crystal display in which the source bus and gate bus driving circuits connected to the source and gate of thin-film-transistors (TFT 13) maintain a TFT display at an active level for a predetermined period after turning OFF the power source. Yasui teaches that after the power supply is turned OFF, each pair of display and counter pixel electrodes are grounded, i.e., discharged to a common potential, within a time period (T) by discharging both electrodes. Yasui col. 6, lns. 3-9. Yasui discloses supplying a common potential to both a display electrode 12a and a counter electrode 12b within a time (T) after the power is turned OFF. Yasui column 6, lines 3 to 6. Yasui discloses that pixel data (D) is set to a logic "0" to clear the

display. Yasui, col. 3, lns. 59-61. The logic "0" pixel data is loaded into a shift register and then applied to the pixels. In particular, Yasui states:

> That is, the source bus driver is designed so that the source bus driver signals S_1 through S_n drop to the common potential within the time T. The display electrode 12a and the counter electrode 12b (the latter being supplied with the voltage E_2) are both supplied with the common potential within the time T, and charges stored in each pixel capacitance in accordance with the display being provided are entirely discharged by the end of the time T. In other words, the time T includes the time necessary for discharging the charges stored in the pixel capacitances. [Yasui, col. 5, lns. 1-11].

Yasui already discloses a method for erasing its display. There is no suggestion or motivation evident in the prior art to discard the Yasui method and replace it with another display erasure method. Contrary to the Action, Tsuboyama does not suggest a modification of Yasui because Tsuboyama does not relate to active matrix TFT displays. Absent a suggestion or motivation evident in the prior art there can be no valid finding of obviouness.

III. TSUBOYAMA DOES NOT SUGGEST MODIFICATION OF YASUI

Because Tsuboyama does not disclose an active matrix having pixel transistors or other pixel switching elements, it is improper to view Tsuboyama as switching pixels ON and OFF as is done in the present invention. Tsuboyama does teach that a constant voltage difference (negative V_4 and zero voltage V_c) is applied across a ferroelectric display to erase the display. This constant voltage difference changes the orientation of liquid crystals in the display. There are no pixels that are turned ON and OFF in the

display disclosed in Tsuboyama. Tsuboyama does not provide a suggestion regarding how to erase pixels in an active matrix display.

It would not have been obvious to modify Yasui's TFT source driver, source driver control circuit or power source control circuit. Tsuboyama primarily discloses a ferroelectric liquid crystal display having a memory function, in which a non-zero voltage is applied to erase the contents of the picture elements of the display. Tsuboyama, col. 1, lns. 9-12 ("The present invention relates to . . . display devices having a memory effect, such as ferroelectric liquid crystal panels."). The "memory effect" described in Tsuboyama relates to irregular orientation of the liquid crystals in ferroelectric LCD display that are caused by a DC voltage applied to the display. Tsuboyama, col. 1, lns. 33-51.

The irregular orientation of liquid crystals that is the subject of Tsuboyama is unrelated to the problem of residually charged pixels in an active matrix display, that is the subject of the present invention. The problems and solutions associated with turning OFF pixel switching elements of active matrix displays are foreign to Tsuboyama's ferroelectric liquid crystal display that has no corresponding switching element. With Tsuboyama's ferroelectric liquid crystal, a voltage is applied to shift and maintain the liquid crystal to a stable display state. A reset pulse (erasing voltage) is applied to erase the display without a distinction as to whether the ON-level signal or the OFF-level signal is applied. A voltage (erasing voltage) is returned to the initial state, and the state is maintained because of a memory property of the liquid crystal. The display erasing

method disclosed in Tsuboyama is particular to ferroelectric displays and not applicable to active matrix displays. Accordingly, a person of ordinary skill in the art would not have looked to Tsuboyama to modify the display erase mechanism disclosed in Yasui.

IV. TSUBOYAMA DOES NOT DISCUSS SPECIFIED LEVEL FOR A SOURCE ENABLE SIGNAL TO ERASE A DISPLAY

The Office Action states that the data side Vc control signal in Figure 5A of Tsuboyama is a source enable (as recited in claim 18) which changes to the selected level (LOW level) during the erase period TE. However, Figure 5A of Tsuboyama describes a data side Vc control signal that is at a LOW level both during the erase period (TE) and during the ordinary display period before power is turned off. The Vc LOW level is not unique to erasing the display after power is off. Because the Vc LOW level is common to operations before and after power is turned off, the Tsuboyama logic control unit 107, upon receiving the data side Vc LOW control signal, must perform the same operation regardless of whether the LOW control signal is applied before or after power is turned off. Because the data side Vc control signal in Tsuboyama is at a LOW level a periods other than after power is off, Tsuboyama does not suggest the claimed source enable signal recited in claim 18 which is at a selecting level "only" after power has been turned off.

In contrast to Tsuboyama, the invention recited in claims 18, 20 and 45 is at the specified level only during the "certain period" which follows the turning OFF the power

source.[1] In the claimed invention, the specified level causes the source driver to apply an OFF voltage to the pixel electrodes which erases the display. With the claimed invention, the source driver, during periods before power off, may output source enable signals that perform other operations using signals other than the recited "specified level". Requiring a "specified level" for the source enable signal that is solely applied after power is turned off ensures that a voltage which is clearly intended to turn off the liquid crystal is applied to the pixel electrodes and the opposite electrode to erase the display. This feature of a "specified level" is patentably distinct from Tsuboyama and Yasui.

V. CONCLUSION

All claims are in good condition for allowance. If any small matter remains outstanding, the Examiner is requested to telephone the undersigned. Prompt reconsideration and allowance of this application is requested.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: _____
Jeffry H. Nelson
Reg. No. 30,481

JHN:glf
1100 North Glebe Road, 8th Floor
Arlington, VA 22201-4714
Telephone: (703) 816-4000
Facsimile: (703) 816-4100

[1] Similarly, new claim 50 requires the source enable signal to include a display erase command.